

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT****Complete if Known**

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First Named Inventor	Eric Hung
Group Art Unit	2186
Examiner Name	
Attorney Docket No.	5201-27500 / 03-1236

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U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code (if known)			
DN		6,618,320		Hasegawa et al.	09-09-2003	
DN		6,154,419		Shakkarwar	11-28-2000	
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DN		6,545,895		Li et al.	04-08-2003	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where	T
DN		"Stub Series Terminated Logic for 2.5 Volts (SSTL 2)", JEDEC Standard, JESD8-9B, May 2002	
DN		"184 Pin PC 1600/2100 DDR SDRAM Unbuffered DIMM Design Specification, JEDEC Standard, Revision 1.1, April 2003	
DN		"TN-46-05, General DDR SDRAM Functionality", Micron Technology, July 2001	

Examiner signature		Date considered	1/26/05
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